A MEASUREMENT METHOD FOR ACCURATE CHARACTERIZATION AND MODELING OF MESFET CHIPS

Don E. Peck
Watkins-Johnson Company, Palo Alto, California 94304

Dean F. Peterson
Electron Physics Laboratory
Department of Electrical and Computer Engineering
The University of Michigan
Ann Arbor, Michigan 48109

ABSTRACT

A straightforward measurement procedure based on a deembedding method and FET unbiased drain RF measurements is presented that produces accurate chip MESFET characteristics. Usefulness of the data is shown by inexpensively obtained MESFET model parameters.

INTRODUCTION

While FET dc and RF terminal characteristics might be derived from physical principles, most users depend on measured data. Obtaining accurate microwave measurements over a broad range of frequencies at the device level can be a problem. The advent of automated network analyzer systems with memory allows highly accurate reference planes to be defined, but extending these references to the device depends on some knowledge of the connecting circuitry. Modeling of this circuitry has often proven inadequate because of the many assumptions regarding connector transitions, unknown lengths of lossy transmission lines, bonding wires, and stray capacitances which usually leads to using expensive computer optimization routines. In this paper, a measurement scheme to overcome these problems is discussed.

Test Fixture Characterizing Procedure

A measurement procedure based on the unterminating[1] technique can be used to find the two-port ABCD-parameter representation of a connecting circuit for any desired frequency provided impedances of known value can terminate the circuit at the same location as the "device" terminals. A varactor with its bias-dependent capacitance (measured at a lower frequency, 1 MHz) can provide the necessary terminations with a minimal amount of physical change in the connecting circuit. Once the connecting circuits are characterized, the value of any load placed at the "device" terminals can then be found by deembedding the load from the connecting circuit.

Once the varactor is removed, a residual resistance due to the varactor's series resistance, R_s, is still a part of the connecting network's ABCD-parameters. This resistance can be found by shorting to ground the end of the connecting circuit by use of a wire similar to that of the varactor bond wire, taking RF measurements of the structure, and then deembedding the resulting measured impedance. The real part of the deembedded impedance will be $-R_s$. By knowing R_s, the connecting circuit's parameters can be corrected. Figure 1 shows a plot of R_s versus frequency. One can see that any one-port microwave device can be measured as discussed. For a two- (or more) port device at least two such connecting circuit characterizations are necessary. One should note that while connecting networks for one-port measurements may be lossy, non-reciprocal, and active, connecting networks used for two- (or more) port devices must be passive and reciprocal.

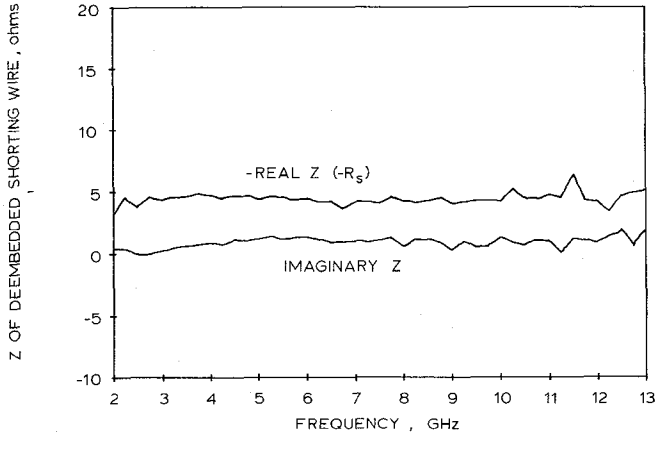


FIGURE 1: MEASUREMENT OF VARACTOR SERIES RESISTANCE. REACTANCE IS THAT OF A SHORT LENGTH OF BONDING WIRE.

FET Measurement Method

When measuring a FET, the resultant deembedded characteristics will include differential input and output lead inductances plus a common terminal bonding lead inductance. The differential inductances are due to the difference between the inductance of the FET bond wire(s)

0149-645X/81/0000-0310$00.75

and the inductance of the varactor bond wire that is a part of the connecting network's parameters. The differential inductance values may be positive or negative depending on whether the FET's bond wires are longer or shorter than the varactor's bond wire.

One can find the values of the differential lead inductances and common terminal inductance by measuring the Z-parameters of the FET in a unbiased drain, "cold chip", state. A "cold chip" model is shown in Figure 2. In the unbiased drain state, the FET is inherently capacitive and resistive, thus any inductive components are due to the lead inductances. Each Z-parameter, having been measured over a wide frequency band, is fitted to a series RLC circuit to extract the inductive components. The inductance values will not change with gate-to-source biasing. Once known, the differential lead inductances are used to correct the deembedded FET characteristics. This results in the availability of accurate FET chip parameters referenced at the bonding pads which can be used for a variety of design and investigative purposes.

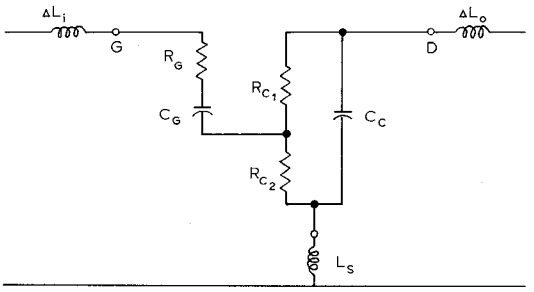


FIGURE 2: UNBIASED DRAIN "COLD CHIP" EQUIVALENT CIRCUIT MODEL OF MESFET.

FET Measurement Example

As an example, this data can be used to determine a FET circuit model that is straightforward, simple, and does not rely on expensive computer optimization methods. By examining the Y-parameter data of a FET chip, the FET can be modeled as the intrinsic two-port circuit shown in Figure 3. With use of straightforward algebraic least squares methods, the values of the circuit elements can be found from the Y-parameters. The circuit parameters values shown in Table 1 are for a NEC 695 FET that was measured over a frequency range of 2-13 GHz. Figure 4 shows a typical calculated fit with the lead inductances taken into account. Figures 5,6,7, and 8 show that comparison of the total calculated Y-parameters to that of the measured Y-parameters.

All the above work was accomplished with the use of an HP-9825 calculator controlled network analyzer system with 24K memory.

REFERENCE

1. R. F. Bauer, and P. Penfield, "Deembedding and Unterminating", IEEE Trans. on Microwave Theory and Techniques, vol. MTT-22, No. 3, pp, 282-288, March 1974

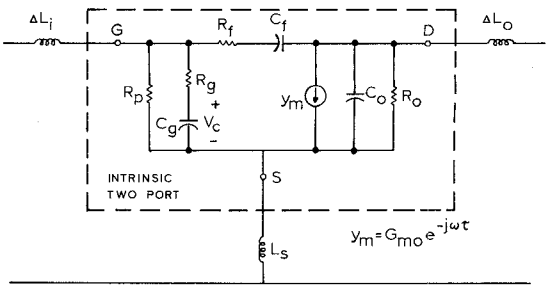
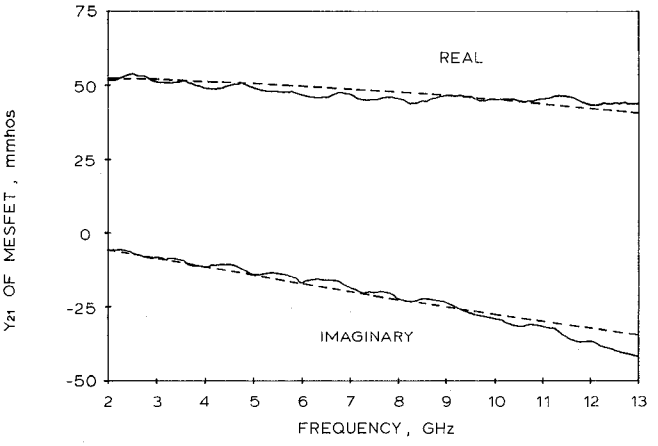


FIGURE 3: COMPLETE EQUIVALENT CIRCUIT MODEL WITH PARASITIC BONDING WIRE INDUCTANCES.

TABLE 1
NEC 695 MESFET COMMON SOURCE CHIP PARAMETERS

Drain Bias (V)	3.00
Gate Bias (V)	-2.50
R_p (ohms)	∞
R_g (ohms)	0.422
C_g (pF)	0.654
R_f (ohms)	-53.27
C_f (pF)	0.0715
G_{mo} (mmho)	58.39
τ (pS)	2.36
R_o (ohms)	211.52
C_o (pF)	0.169
ΔL_i (nH)	-0.34 *
ΔL_o (nH)	-0.017 *
L_s (nH)	0.125
Frequency	2 GHz - 13 GHz

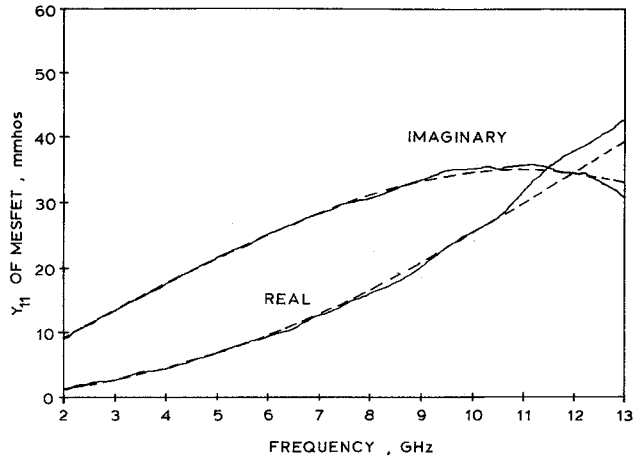
* Negative inductance is implied because the FET input and output bonding wires are shorter than the varactor bonding wire and the input had two bond wires.



----- Calculated Y_{21} from Intrinsic Model

——— Deembedded Measured Y_{21}

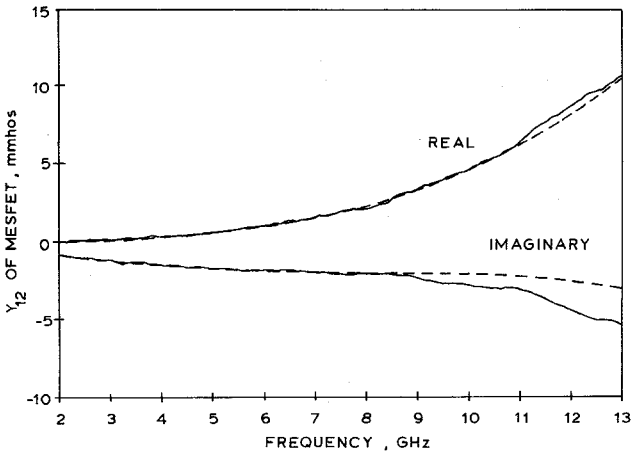
FIGURE 4: MEASURED AND FITTED VALUES OF Y_{21} FOR AN NEC 695 MESFET WITH INDUCTANCES ΔL_i, ΔL_o, AND L_s STRIPPED FROM THE MEASURED DATA.



----- Calculated Y_{11} from Extrinsic Model Including ΔL_i, ΔL_o, and L_s.

——— Unaltered Measured Y_{11}.

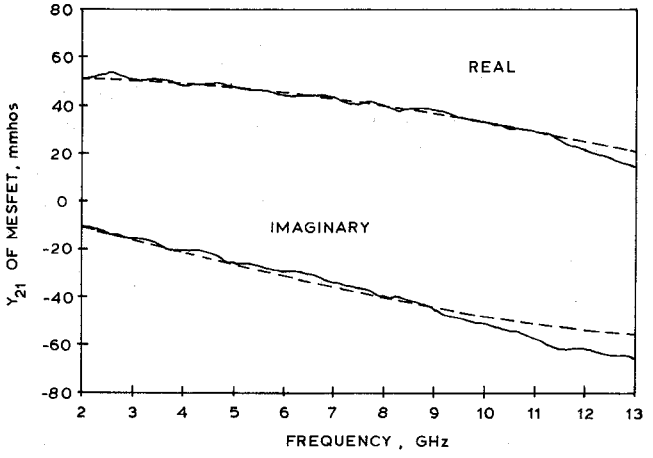
FIGURE 5: COMPARISON OF Y_{11} CALCULATED FROM THE EXTRINSIC MODEL TO UNALTERED MEASURED Y_{11} DATA.



----- Calculated Y_{12} from Extrinsic Model Including ΔL_i, ΔL_o, and L_s.

——— Unaltered Measured Y_{12}.

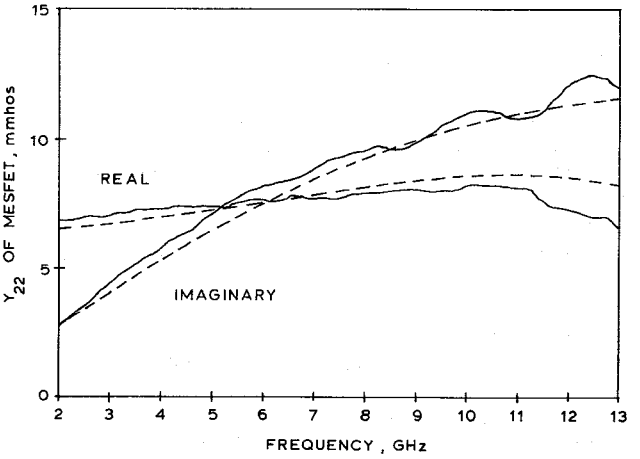
FIGURE 6: COMPARISON OF Y_{12} CALCULATED FROM THE EXTRINSIC MODEL TO UNALTERED MEASURED Y_{12} DATA.



----- Calculated Y_{21} from Extrinsic Model Including ΔL_i, ΔL_o, and L_s.

——— Unaltered Measured Y_{21}.

FIGURE 7: COMPARISON OF Y_{21} CALCULATED FROM THE EXTRINSIC MODEL TO UNALTERED MEASURED Y_{21} DATA.



----- Calculated Y_{22} from Extrinsic Model Including ΔL_i, ΔL_o, L_s.

——— Unaltered Measured Y_{22}.

FIGURE 8: COMPARISON OF Y_{22} CALCULATED FROM THE EXTRINSIC MODEL TO UNALTERED MEASURED Y_{22} DATA.